MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Computer Organization**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**COMP1203**				
ECTS Credits	**8**				
SWL (hr/sem)	**200**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	CS		**College**	College of Sciences	
Module Leader	Dr. Safaa H. Shwail		**e-mail**	safaa.husseinshwail@nahrainunive.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	Ph.D.	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date	01/06/2023		**Version Number**	1.1	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	Computer	**Semester**	1
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. Learning the Numbering Systems and the main Operations on them. 2. Learning the Processor and its architecture 3. Exploring the Intel 80x86 Base Architecture I 4. Knowing the Instruction Set Architecture 5. Learning the Addressing Modes and the number of addresses 6. Recognizing the Characteristics of Memory Systems 7. Exploring the Memory Hierarchy and the difference between memory types.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Binay System, Addition, Subtraction. 2. The main components of the Processor and its architecture 3. Processor level architecture 4. CPU level architecture 5. Intel 80x86 Base Architecture: Execution Unit 6. Intel 80x86 Base Architecture: Bus Interface Unit 7. Memory versus I/O Ports 8. Instruction Set Architecture 9. Addressing Modes and number of addresses 10. Memory Locations and Operations 11. Memory Hierarchy 12. Characteristics of Memory Systems 13. CACHE MEMORY PRINCIPLES 14. SEMICONDUCTOR MAIN MEMORY 15. Types of RAM 16. Types of ROM
Indicative Contents المحتويات الإرشادية	Learning how to convert decimal numbers to binary and vice versa, applying the addition and the subtraction and multiplication on the binary numbers. Learning the Processor and its architecture: Bus, Registers, Flags, Buffers, Stack, and I/O ports. Exploring processor and CPU level architecture. Exploring Execution unit of the Intel 80x86 Base Architecture: the general-purpose registers, address registers, flags, and Internal buses. Exploring Bus Interface Unit of the Intel 80x86 Base Architecture: Segment Addressing, Instruction Queue, and Memory versus I/O Ports. Knowing the Instruction Set Architecture: Data Movement Instructions, Arithmetic and Logical Instructions, Sequencing Instructions, and Input/Output Instructions.

	Learning the Addressing Modes and the number of addresses: Immediate Mode, Direct (Absolute) Mode, Indirect Mode, Indexed Mode, Relative Mode, Autoincrement Mode, and Autodecrement Mode. Recognizing the Characteristics of Memory Systems and Exploring the Memory Hierarchy and the difference between memory types: method of accessing units of data, CACHE MEMORY PRINCIPLES, SEMICONDUCTOR MAIN MEMORY, types of RAM, and types of ROMs.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is by explaining lectures in an interactive way by letting the students to participate in the presenting through questions and answers while at the same time refining and expanding their critical thinking skills. This will be achieved through classes and labs.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	63	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	7
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	37	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	6
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	100		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	4	10% (10)	2,5,8,12	All
	Assignments	2	5% (5)	5,10	All

	Projects / Lab.	1	15% (15)	Continuous	All
	Report	1	10% (10)	10	All
Summative assessment	**Midterm Exam**	2 hr	10% (10)	7,14	All
	Final Exam	3hr	50% (50)	15	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Binary System and Operations
Week 2	Processor and its architecture
Week 3	Intel 80x86 Base Architecture I
Week 4	Intel 80x86 Base Architecture I (cont.)
Week 5	Intel 80x86 Base Architecture II
Week 6	Intel 80x86 Base Architecture II (cont.)
Week 7	Intel 80x86 Base Architecture II (cont.)
Week 8	Mid-term Exam 1
Week 9	Instruction Set Architecture
Week 10	Instruction Set Architecture (cont.)
Week 11	Addressing Modes
Week 12	Addressing Modes (cont.)
Week 13	Memory Hierarchy
Week 14	Memory Hierarchy (cont.)
Week 15	Mid-term Exam 2
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Introduction
Week 2	Lab 2: Movement Instructions
Week 3	Lab 3: Movement Instructions

Week 4	Lab 4: Movement Instructions
Week 5	Lab 5: Arithmetic Instructions
Week 6	Lab 6: Arithmetic Instructions
Week 7	Lab 7: Arithmetic Instructions
Week 8	Mid-Term Exam 1
Week 9	Lab 8: Logic Instructions
Week 10	Lab 9: Logic Instructions
Week 11	Lab 10: Logic Instructions
Week 12	Lab 11: Sequencing and Jump Instructions
Week 13	Lab 12: Sequencing and Jump Instructions
Week 14	Lab 13: Sequencing and Jump Instructions
Week 15	Mid-Term Exam 2

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Computer Organization and Architecture Designing for Performance, 8th Edition, by William Stallings, 2010	No
Recommended Texts	Computer Systems; A Programmer's Perspective - 2nd Edition, 2011	No
Recommended Texts	Fundamentals of Logic Design, 6th edition 2010	No

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.